SUPPLEMENT

# MOSTEK®

## 4096x1-BIT DYNAMIC RAM

# MK4015 (J/N)

### FEATURES

- ☐ Recognized industry standard 16-pin configuration from Mostek
- ☐ 250ns access time, 380ns cycle
- ☐ Output data latched and valid into next cycle
- ☐ Low Power: 462mW active (max)
  38mW standby (max)
- ☐ Improved performance with "gated $\overline{CAS}$", "$\overline{RAS}$ only" refresh, and Read-Modify-Write
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Input latches for addresses, chip select and data in
- ☐ Three-state TTL compatible output

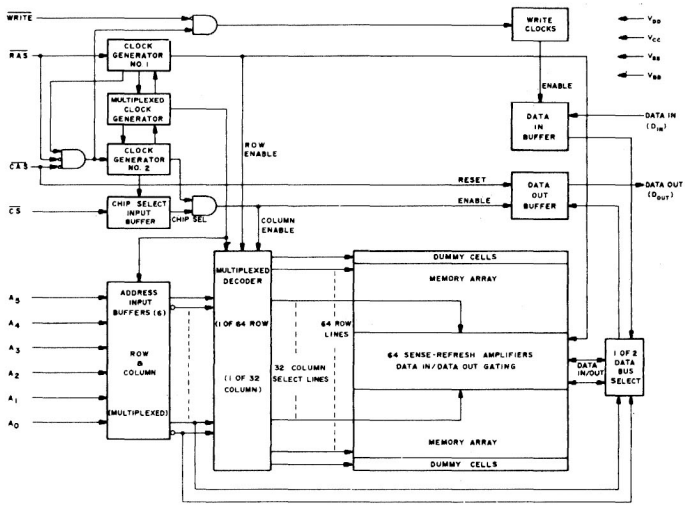
### DESCRIPTION

The MK 4015 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4015 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4015 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

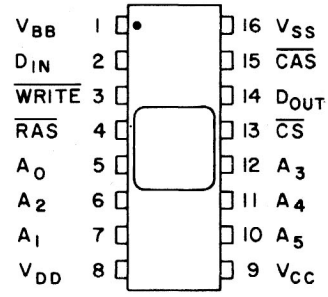
A unique multiplexing and latching technique for the address inputs permits the MK 4015 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4015 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, and $\overline{RAS}$-only refresh cycles are available with the MK 4015.

### FUNCTIONAL DIAGRAM




### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| $A_0$-$A_5$ | ADDRESS INPUTS |
| $\overline{CAS}$ | COLUMN ADDRESS STROBE |
| $\overline{CS}$ | CHIP SELECT |
| $D_{IN}$ | DATA IN |
| $D_{OUT}$ | DATA OUT |
| $\overline{RAS}$ | ROW ADDRESS STROBE |
| $\overline{WRITE}$ | READ/WRITE INPUT |
| $V_{BB}$ | POWER (−5V) |
| $V_{CC}$ | POWER (+5V) |
| $V_{DD}$ | POWER (+ 12V) |
| $V_{SS}$ | GROUND |

## ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to $V_{BB}$ ..... −0.5V to +20V
Voltage on $V_{DD}$, $V_{CC}$ relative to $V_{SS}$ ..... −1.0V to +15V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS} > 0$) ..... 0V
Operating temperature, $T_A$ (Ambient) ..... 0°C to +55°C
Storage temperature (Ambient)(Ceramic) ..... −65°C to + 150°C
Storage temperature (Ambient)(Plastic) ..... −55°C to + 125°C
Short Circuit Output Current ..... 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS [4]

(0°C ≤ $T_A$ ≤ 55°C) [1]

| | PARAMETER | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 11.4 | 12.0 | 12.6 | volts | 2 |
| $V_{CC}$ | Supply Voltage | 4.5V | 5.0 | 5.5 | volts | 2,3 |
| $V_{SS}$ | Supply Voltage | 0 | 0 | 0 | volts | 2 |
| $V_{BB}$ | Supply Voltage | −4.5 | −5.0 | −5.5 | volts | 2 |
| $V_{IHC}$ | Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ | 3.0 | | 7.0 | volts | 2 |
| $V_{IH}$ | Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ | 3.0 | | 7.0 | volts | 2 |
| $V_{IL}$ | Logic 0 Voltage, all inputs | −1.0 | | .65 | volts | 2 |

## DC ELECTRICAL CHARACTERISTICS [4]

(0°C ≤ $T_A$ ≤ 55°C)[1] ($V_{DD}$ = 12.0V ± 5%; $V_{CC}$ = 5.0V ± 10%; $V_{SS}$ = 0V; $V_{BB}$ = −5.0V ± 10%)

| | PARAMETER | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $I_{DD1}$ | Average $V_{DD}$ Power Supply Current | | | 35 | mA | 5 |
| $I_{DD2}$ | Standby $V_{DD}$ Power Supply Current | | | 3 | mA | 8 |
| $I_{DD3}$ | Average $V_{DD}$ Power Supply Current during "$\overline{RAS}$ only" cycles | | | 25 | mA | |
| $I_{CC}$ | $V_{CC}$ Power Supply Current | | | | mA | 6 |
| $I_{BB}$ | Average $V_{BB}$ Power Supply Current | | | 150 | μA | |
| $I_{I(L)}$ | Input Leakage Current (any input) | | | 10 | μA | 7 |
| $I_{O(L)}$ | Output Leakage Current | | | 10 | μA | 8,9 |
| $V_{OH}$ | Output Logic 1 Voltage @ $I_{OUT}$ = −5mA | 2.4 | | | volts | |
| $V_{OL}$ | Output Logic 0 Voltage @ $I_{OUT}$ = 3.2mA | | | 0.4 | volts | |

NOTES

1. $T_A$ is specified for operation at frequencies to $t_{RC} \geq t_{RC}$ (min).
2. All voltages referenced to $V_{SS}$.
3. Output voltage will swing from $V_{SS}$ to $V_{CC}$ when enabled, with no output load. For purposes of maintaining data in standby mode, $V_{CC}$ may be reduced to $V_{SS}$ without affecting refresh operations or data retention. However, the $V_{OH}$ (min) specification is not guaranteed in this mode.
4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
5. Current is proportional to cycle rate. $I_{DD1}$ (max) is measured at the cycle rate specified by $t_{RC}$ (min). See figure 1 for $I_{DD1}$ limits at other cycle rates.
6. $I_{CC}$ depends on output loading. During readout of high level data $V_{CC}$ is connected through a low impedance (135Ω typ) to Data Out. At all other times $I_{CC}$ consists of leakage currents only.
7. All device pins at 0 volts except $V_{BB}$ which is at −5 volts and the pin under test which is at +10 volts.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. 0V ≤ $V_{OUT}$ ≤ + 10V.
10. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

11. A.C. measurements assume $t_T$ = 5ns.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS[4,11,17]

(0°C ≤ TA ≤ 55°C)[1] (VDD = 12.0V ± 5%, VCC = 5.0V ± 10%, VSS = OV, VBB = -5.0V ± 10%)

| | PARAMETER | MK4015 MIN | MK4015 MAX | Units | Notes |
|---|---|---|---|---|---|
| $t_{RC}$ | Random read or write cycle time | 380 | | ns | |
| $t_{RWC}$ | Read write cycle time | 395 | | ns | |
| $t_{RMW}$ | Read modify write cycle time | 470 | | ns | |
| $t_{RAC}$ | Access time from row address strobe | | 250 | ns | 13,15 |
| $t_{CAC}$ | Access time from column address strobe | | 165 | ns | 14,15 |
| $t_{OFF}$ | Output buffer turn-off delay | | 60 | ns | |
| $t_{RP}$ | Row address strobe precharge time | 120 | | ns | |
| $t_{RAS}$ | Row address strobe pulse width | 250 | 4000 | ns | |
| $t_{RSH}$ | Row address strobe hold time | 165 | | ns | |
| $t_{CAS}$ | Column address strobe pulse width | 165 | 4000 | ns | |
| $t_{CSH}$ | Column address strobe hold time | 250 | | ns | |
| $t_{RCD}$ | Row to column strobe delay | 35 | 85 | ns | 16 |
| $t_{ASR}$ | Row address set-up time | 0 | | ns | |
| $t_{RAH}$ | Row address hold time | 35 | | ns | |
| $t_{ASC}$ | Column address set-up time | 0 | | ns | |
| $t_{CAH}$ | Column address hold time | 75 | | ns | |
| $t_{AR}$ | Column address hold time referenced to RAS | 160 | | ns | |
| $t_{CSC}$ | Chip select set-up time | 0 | | ns | |
| $t_{CH}$ | Chip select hold time | 75 | | ns | |
| $t_{CHR}$ | Chip select hold time referenced to RAS | 160 | | ns | |
| $t_{T}$ | Transition time (rise and fall) | 3 | 50 | ns | 17 |
| $t_{RCS}$ | Read command set-up time | 0 | | ns | |
| $t_{RCH}$ | Read command hold time | 0 | | ns | |
| $t_{WCH}$ | Write command hold time | 75 | | ns | |
| $t_{WCR}$ | Write command hold time referenced to RAS | 160 | | ns | |
| $t_{WP}$ | Write command pulse width | 75 | | ns | |
| $t_{RWL}$ | Write command to row strobe lead time | 100 | | ns | |
| $t_{CWL}$ | Write command to column strobe lead time | 100 | | ns | |
| $t_{DS}$ | Data in set-up time | 0 | | ns | 18 |
| $t_{DH}$ | Data in hold time | 75 | | ns | 18 |
| $t_{DHR}$ | Data in hold time referenced to RAS | 160 | | ns | |
| $t_{CRP}$ | Column to row strobe precharge time | 0 | | ns | |
| $t_{RFSH}$ | Refresh period | | 1 | ms | |
| $t_{WCS}$ | Write command set-up time | 0 | | ns | 19 |
| $t_{CWD}$ | CAS to WRITE delay | 90 | | ns | 19 |
| $t_{RWD}$ | RAS to WRITE delay | 175 | | ns | 19 |
| $t_{DOH}$ | Data out hold time | 4 | | μs | |

Notes Continued

13. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
14. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
15. Measured with a load circuit equivalent to 2 TTL loads and 100pF
16. Operation within the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
17. $V_{IHC}$ (min) or $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IHC}$ or $V_{IH}$ and $V_{IL}$.
18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
19. $t_{WCS}$, $t_{CWD}$, and $t_{RWD}$ are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

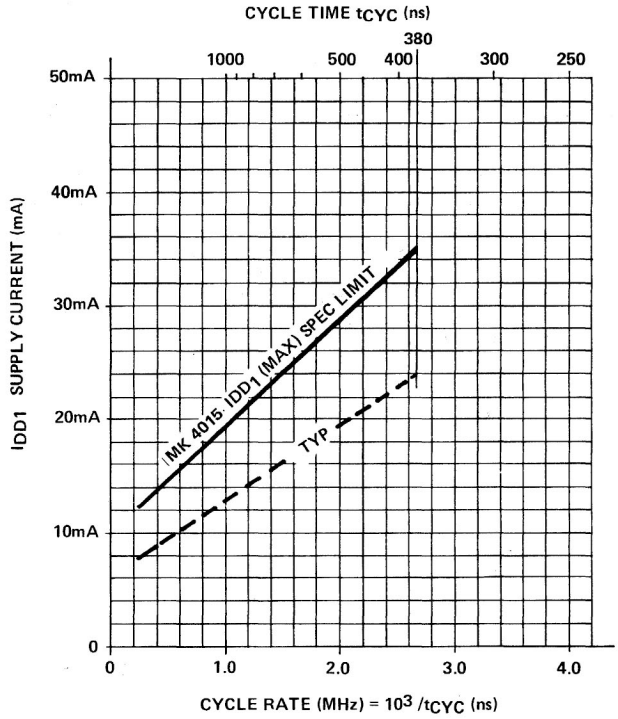
## AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 55°C$) ($V_{DD}$ = 12V ± 5%; $V_{SS}$ = 0V; $V_{BB}$ = –5.0V ± 10%)

| | PARAMETER | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $C_{I1}$ | Input Capacitance ($A_0$-$A_5$), $D_{IN}$, $\overline{CS}$ | 4 | 5 | pF | 10 |
| $C_{I2}$ | Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ | 8 | 10 | pF | 10 |
| $C_O$ | Output Capacitance ($D_{OUT}$) | 5 | 7 | pF | 8,10 |

## MAXIMUM $I_{DD1}$ vs. CYCLE RATE

**Figure 1**




**SUPPLEMENT - To be used in conjunction with MK4027(P/J/N)-1/2/3 data sheet.**